Notice of Allowability	Application No.	Applicant(s)	
	10/707,027	WU ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the papers submitted on 16 November 2003*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Amendment

2. The application has been amended as follows:

Abstract of the Disclosure

The abstract has been replaced with the following:[1]

~~This invention discloses a~~ A method for fabricating a deep trench capacitor. A substrate is provided~~. A~~ having a pad oxide layer and a pad nitride layer ~~are~~ stacked on a main surface ~~of the substrate~~ thereof. A deep trench is etched into the substrate through the pad oxide layer and the pad nitride layer. ~~A doped area is formed at the lower portion of the deep trench serving as the first electrode of the trench capacitor.~~ A node dielectric is coated on the interior surface of the deep trench. ~~A first polysilicon layer is deposited in the deep trench and is then recessed to a first depth.~~ A silicon spacer layer is formed on the sidewall of the deep trench over the node dielectric. An upper portion of the silicon spacer layer is doped with dopants such as BF_2. The ~~un-doped~~ undoped portion of the silicon spacer layer is selectively removed to expose a portion of the

node dielectric. The exposed node dielectric is stripped off to expose the substrate. The remaining node dielectric covered by the doped silicon spacer layer forms a protection spacer for protecting the pad oxide layer from corrosion during the subsequent etching processes.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance: the prior art of record does not anticipate, teach or suggest a method for fabricating a trench capacitor of DRAM devices substantially as claimed. As evidenced by Applicant's admitted prior art, the following process steps for fabricating a trench capacitor in a DRAM device are known: etching a deep trench into a semiconductor substrate, the substrate having a pad oxide layer and a pad nitride layer stacked thereon; doping the deep trench to form a buried doped plate in the semiconductor substrate adjacent to a lower portion of the deep trench; forming a node dielectric layer on interior surface of the trench; depositing a first conductive layer on the node dielectric layer inside the trench; and recessing the first conductive layer to a first depth in the deep trench. However, the prior art of record does not anticipate, teach or suggest a method for fabricating a trench capacitor substantially as claimed, wherein the method comprises at least the steps of: depositing a silicon layer on the node dielectric layer on sidewall of the deep trench; locally ion doping an upper portion of the spacer silicon layer; selectively removing the non-doped silicon

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[1] The abstract in an application filed under 35 U.S.C. 111 may not exceed 150 words in length

layer to expose the node dielectric layer; removing the exposed node dielectric layer to expose a silicon surface inside the deep trench, and simultaneously forming a dielectric spacer protecting the pad oxide layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
19 September 2005

EXAMINER

(37 CFR 1.72(b)).